IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

James D.Y. COLLIER et al.

Serial No.: 09/618,296

Filed: July 18, 2000

For: VARIABLE OSCILLATOR

Examiner: David Q. Nguyen

Group Art Unit: 2681

DECLARATION UNDER 37 C.F.R. § 1.131

We, James Digby Yarlet Collier and Ian Michael Sabberton, the inventors in the above-captioned patent application, hereby respectfully submit this declaration to overcome the Endo et al. prior art reference relied upon by the Examiner in the Office action of October 24, 2002 specifically, U.S. Patent No. 6,172,576 to Endo et al., having a filing date of April 2, 1999. To that end, we hereby declare as follows:

1. We incorporate herein by reference our prior declaration under 37 CFR § 1.131 filed in the subject application on 24 April 2003, which establishes conception of the claimed invention prior to April 2, 1999.

2. During the period of time the subject matter of this application was being developed, we were employed by Cambridge Silicon Radio, Ltd. (CSR) of Cambridge, England, the assignee of this application.

3. The subject matter of this application was developed in conjunction with the CSR single chip bluetooth device known as BlueCore 01b.

4. A laboratory notebook was kept by us in connection with the development of the subject matter of this application.

5. Copies of certain pages of that notebook, which were prepared between a date prior to April 2, 1999 and July 19, 1999, the filing date of UK Patent Application No. 9916907.0, which is claimed as priority under 35 U.S.C. § 119 ("the priority application"), are attached to this declaration at Exhibit A.

6. These pages demonstrate that we acted with due diligence toward the development of the subject matter of the claims of this application from a time prior to April 2, 1999 through July 19, 1999, the filing date of the priority application. In particular, the attached handwritten notes reflect that continuous design development work and experimental testing were performed between April 2, 1999 and July 19, 1999.

7. Moreover, the pages show various drawings illustrating various configuration options for a variable oscillator that were conceived and evaluated. These drawings correspond to the embodiments of the invention as shown in Figs. 1-5 of the present application.

DECLARATION UNDER 37 C.F.R. § 1.68

All statements made herein of our own knowledge are true and all statements made on information and belief are believed to be true. We understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of this application or any patent issuing thereon.

James D. Y. Collier

14 February 2005

Date

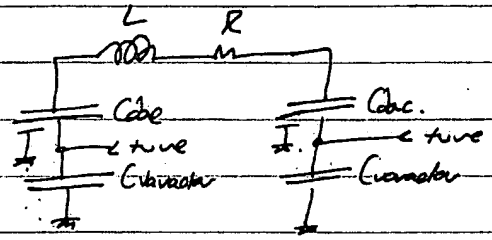
Ian Michael Sabberton

14th February 2005.

Date

VCO (pair) Trim Structure. 18 March 99.

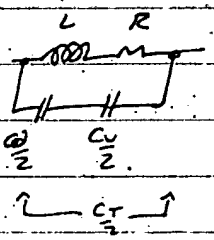
Circuit:-



Tolerances: require constant loop gain over process.

$$\Rightarrow \frac{\partial \omega}{\partial V_{tune}} = \text{constant}.$$

analysis: model network as



$$\left\{ C_T = \frac{C_\omega . C_v}{C_\omega + C_v} \right.$$

$$\omega^2 = \frac{2.L - R^2 C_T}{C_T L^2}$$

$$= \frac{2\frac{L}{C_T} - R^2}{L^2}.$$

$$\frac{\partial \omega}{\partial C_T} = \frac{1}{2}\left(2\frac{\frac{L}{C_T} - R^2}{L^2}\right)^{-1/2}\left(\frac{-2}{L C_T^2}\right)$$

$$= \frac{-1}{C_T^2 . \left(\frac{2L}{C_T} - R^2\right)^{1/2}} \Rightarrow \frac{\partial \omega}{\partial C_T} = \frac{-1}{C_T^2 . \omega . L}.$$

$\left(\frac{2L}{C_T} - R^2\right)^{1/2} = \omega . L.$

$$\frac{\partial \omega}{\partial C_v} = \frac{\partial \omega}{\partial C_T}\frac{\partial C_T}{\partial C_v}. \qquad \frac{\partial C_T}{\partial C_v} = \frac{C_\omega^2}{(C_\omega + C_v)^2}$$

$$\therefore \frac{\partial \omega}{\partial C_v} = \frac{-C_\omega^2}{(C_\omega + C_v)^2} \cdot \frac{1}{\omega . L} \cdot \frac{(C_\omega + C_v)^2}{C_\omega^2 C_v^2} = \frac{-1}{\omega . L . C_v^2}$$

$\Rightarrow$ for constant $\frac{\partial \omega}{\partial C_v}$ at fixed ω requires $L \propto \frac{1}{C_v^2}$.

PTO

VCO Trim Continued.

have $\frac{\partial \omega}{\partial C_V} = \frac{-1}{\omega \cdot L \cdot C_V^2}$

want constant $\frac{\partial \omega}{\partial V_{tune}}$, ⇒ require knowledge about $\frac{\partial C_V}{\partial V_{tune}}$ for varactor.

i, ideal(ish) case. $C_V = \frac{C_{V0}}{(1 - V_F/\phi)^n}$ ← zero bias capacitance; ↖ assume $= 1/2$.

then $\frac{\partial C_V}{\partial V_F} = \frac{C_{V0}}{2\phi(1 - V_F/\phi)^{3/2}}$

($V_F = V_{tune}$)

$$\Rightarrow \frac{\partial \omega}{\partial V_{tune}} = \frac{C_{V0}}{2\phi(1 - V_F/\phi)^{3/2}} \cdot \frac{1}{\omega \cdot L} \cdot \frac{\left((1 - V_F/\phi)^{1/2}\right)^2}{C_{V0}^2}$$

$$= \frac{-1}{2 C_{V0} \cdot \phi \cdot (1 - \frac{V_{tune}}{\phi})^{1/2} \cdot \omega \cdot L}$$

if $V_{tune} = 1V$ at L_{nom}, assume $\phi = 0.5V$.

what is V_{tune} at $L = +10\%$ for same $\frac{\partial \omega}{\partial V_{tune}}$?

$$\frac{\partial \omega}{\partial V_{tune}} \propto \frac{-1}{L \cdot (1 - \frac{V_{tune}}{\phi})^{1/2}}$$

$\therefore$ if $L = +10\%$ $V_{tune} \leq 0.7V$.

⇒ ↙ C_V smaller = larger ⇒ C_V = smaller for same ω.

ii, ST varactor model. $\phi \doteq 0.5V$

$n \doteq 1/3$.

$$\frac{\partial C_V}{\partial V_F} = \frac{C_{V0}}{3\phi\left(1-\frac{V_F}{\phi}\right)^{4/3}}.$$

$$\Rightarrow \frac{\partial \omega}{\partial V_{true}} = \frac{C_{V0}}{3\phi\left(1-\frac{V_F}{\phi}\right)^{4/3}} \cdot \frac{-1}{\omega \cdot L} \cdot \frac{\left(1-V_F/\phi\right)^{2/3}}{C_{V0}^{2}}$$

$$\frac{\partial \omega}{\partial V_{true}} = \frac{-1}{3 C_{V0}\phi\left(1-V_F/\phi\right)^{2/3} \cdot \omega \cdot L}$$

{ if $V_{TRUE} = 1V$ at L_{nom}, what is V_{TRUE} at $L = +10\%$.

$$\frac{\partial \omega}{\partial V_{true}} \propto \frac{-1}{L\left(1-\frac{V_{true}}{\phi}\right)^{2/3}}$$

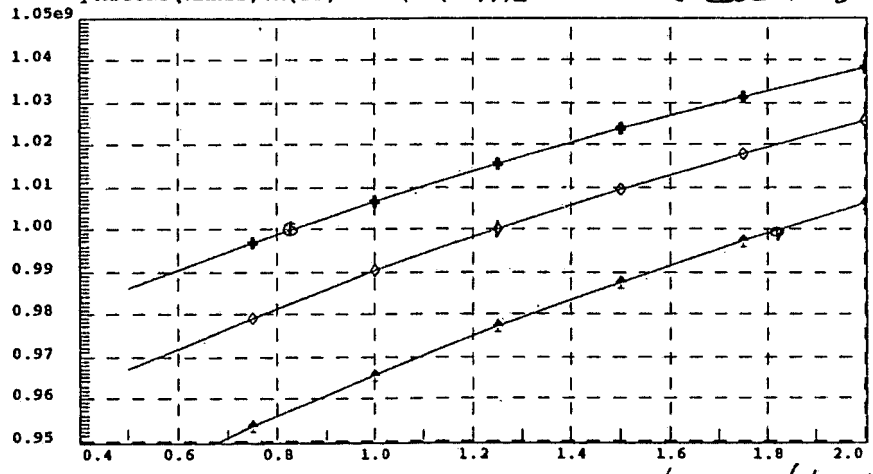
$\therefore$ if $L = +10\%$ $V_{TRUE} = 0.69\ V$.

$\Rightarrow$ C varactor is at $+$ [illegible]%, L at $+10\%$ $\Rightarrow$ CO low.

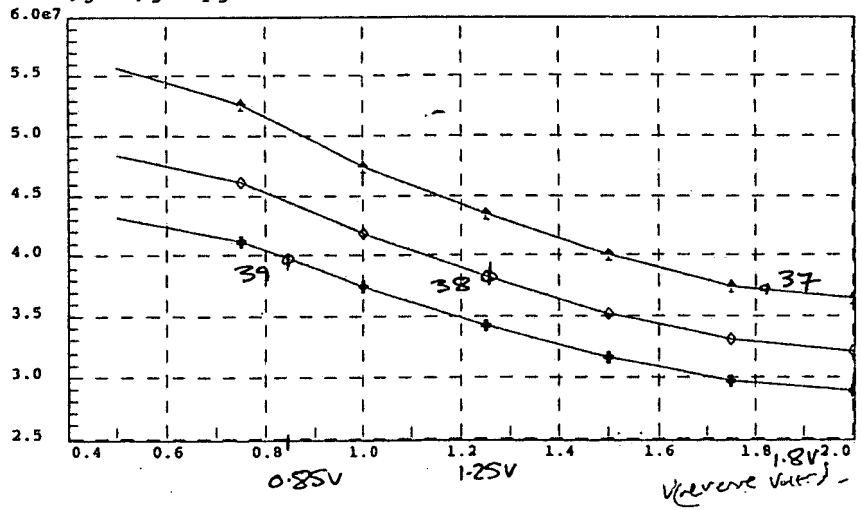
(-10%, $V_{TRUE} = 1.26V$, C varactor at $-$ [illegible]% $\Rightarrow$ CO high.

```
* simulation to check constant dfreq/dVbias of varactor tuned pierce
* oscillator


*  circuit :-
*
*           --- ind ----
*            |        |
*           Ct1      Ct2   - core  ≃8p
*            |        |
*           xCv1     xCv2   ≃15p
*            |        |
*           Gnd      Gnd
*
*
* expect  dfreq/dCv = -1 / (Cv^2*Fres*Lind)
*       freq and Fres (resonant freq) in rad/sec



* inductor Q of 10 at 1GHz
l1  t1 n1  IND
r1  n1 t2  6
.param  IND=10n
* capacitor networks 5pF eq each (2.5p eff load across ind)
ct1  t1 nc1  CDAC
xcv1  0 nc1 0  va148m1
ct2  t2 nc2  CDAC
xcv2  0 nc2 0  va148m1
.param  CDAC=8p
*
vtune  tune 0  BIAS
.param  BIAS=0
rtune1  nc1 tune  10e3
rtune2  nc2 tune  10e3
* dummies
rd3  t1 0  1e9

* drive
idrive  t1 t2  0  ac 1



.ac  lin 5000 750e6 1.25e9
.step param  BIAS 0.5 2.0 0.25

.plot ac  vdb(t1) vdb(t2)
.extract  xycond(xaxis, vm(t1) >= max(vm(t1)))

.lib  /home/csrcad/process/st/bicmos_0u35/eldo/capacitor.lib  varactor_typ



.alter
.param  IND=11n
.param  CDAC=6.6p


.alter
.param  IND=9n
.param  CDAC=10.3p
```

◇ XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_1:2 typ Cdac typ
✚ XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_2:2 L + 10% Cdac -23%
‡ XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_3:2 L - 10% Cdac +27%



◇ gr1 ✚ gr2 ‡ gr3



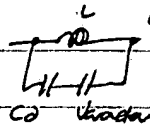
Constant VCO constant for VCO inductor over ± 10% range.
achieved by adjusting varactor operating point and (fixed per sim)
differing capacitance

Target: frequency 1.225GHz ± 20MHz pull.

KVCO 10 MHz/V.

want KVCO independent of channel. L ≈ 5 nH.

from previous page: $\frac{d\omega}{dtune} = \frac{-1}{3C_0\phi\left(1-\frac{V_t}{\phi}\right)^{3/2}\cdot\omega_0 L}$ for varactor with $m = \frac{1}{3}$ (like ST part).

for 

⇒ for 10 MHz/V C_0 = 69 pF @ V_t = −1V.

$C_{varactor}$ @ −1V = 48 pF.

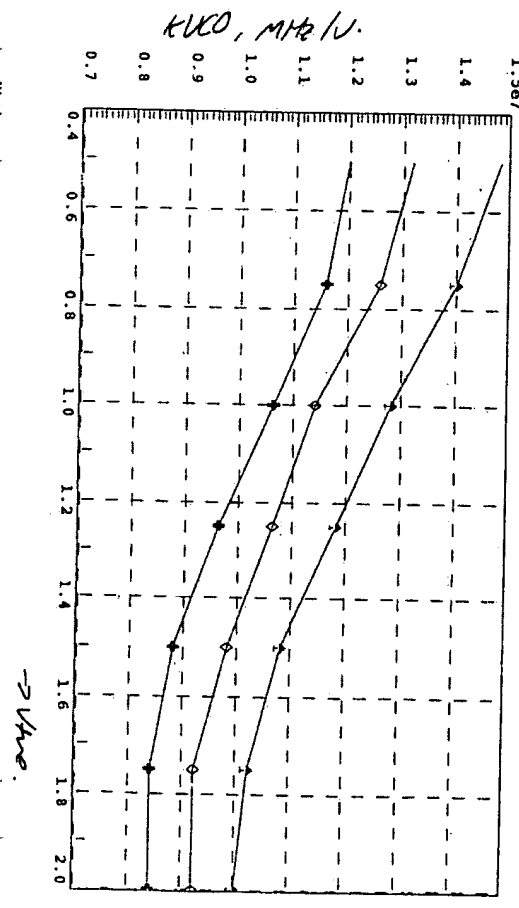
⇒ C_d = 3.65 pF.

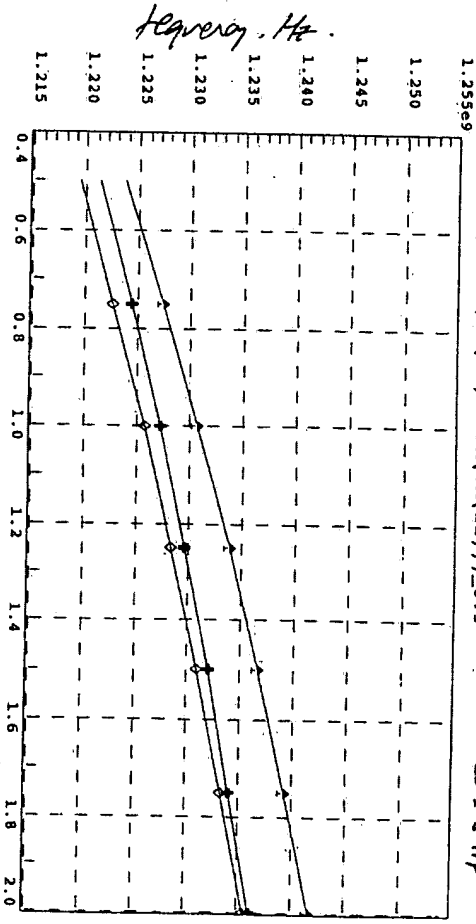
---

change L to 5.5 nH ⇒ +10% . if Varactor at 1V still ⇒ $\frac{d\omega}{dtune}$ at 90%.

" 4.5 nH ⇒ −10% " " " 110%.

continued below.



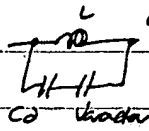


Target: frequency 1.225GHz ± 20MHz pull.

KVCO 10 MHz/V.

want KVCO independent of channel: $L \cong 5\,nH$.

from previous page: $\frac{d\omega}{dtune} = \frac{-1}{3C_0\phi\left(1-\frac{V_t}{\phi}\right)^{3/2}\cdot\omega_0 L}$ for varactor with $m = 1/3$ (like ST part).

for 

⇒ for 10MHz/V $C_0 = 69\,pF$ @ $V_t = -1V$.

Varactor @ $-1V = 48\,pF$.

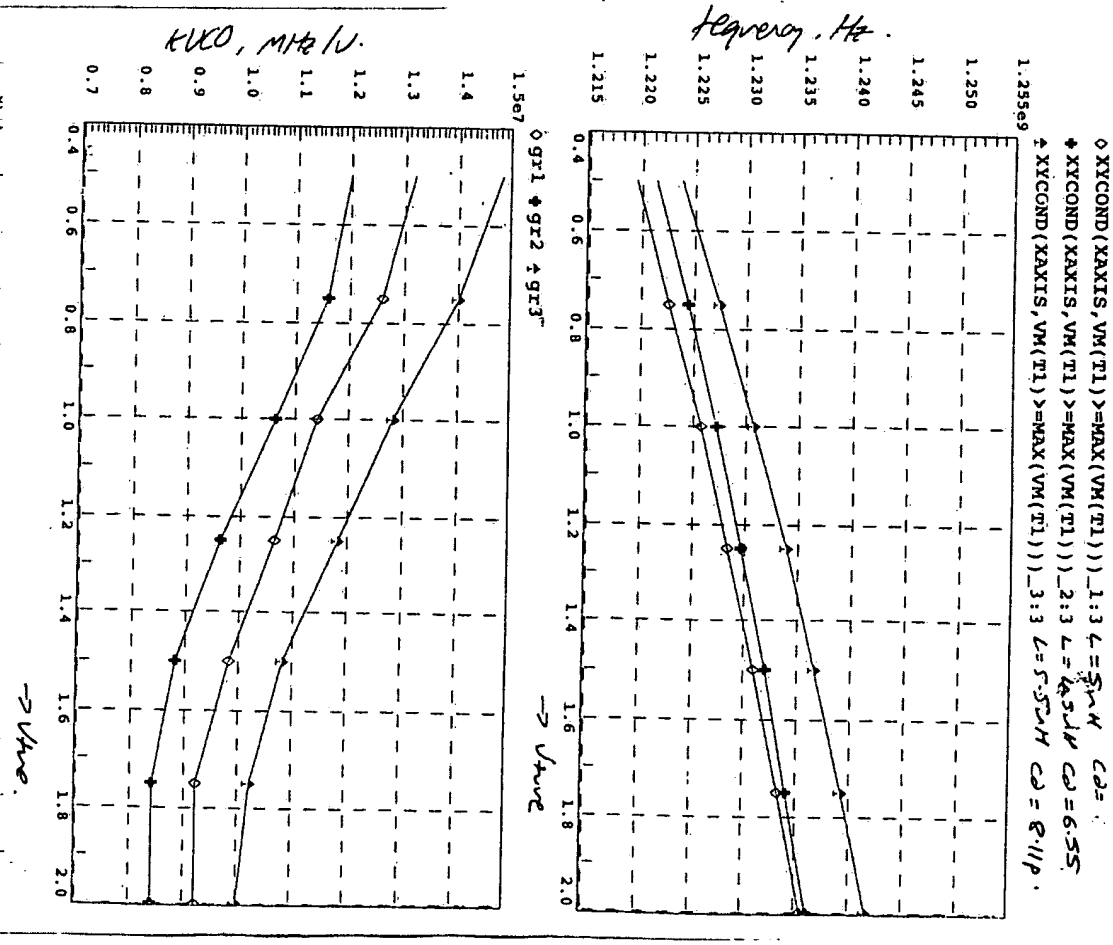
⇒ $C_d = 3.65\,pF$.

---

change L to 5.5nH ⇒ +10% . if Varactor at 1V still ⇒ $\frac{d\omega}{dtune}$ at 90%.

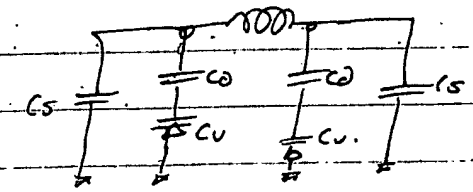
" 4.5nH ⇒ −10% " " " 110%.

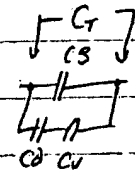
continued below.



VCO continued.

Previous showed good performance although the need for a large varactor, 2x140pF is precise configuration. Try :—





$$\rightarrow C_T = \frac{C_s(C_d+C_v)+C_dC_v}{C_d+C_v}$$

replacing the fact that there are two of the above network in series :—

$$\frac{dC_T}{dC_v} = \frac{C_d^2}{(C_d+C_v)^2}$$

$$\frac{d\omega}{dC_v} = \frac{C_d^2}{\omega \cdot L \cdot (C_s(C_d+C_v)+C_dC_v)^2}$$

assuming $C_v \gg C_s, C_d$.

$$\Rightarrow \frac{C_d^2}{\omega \cdot L \cdot C_v^2 (C_s+C_d)^2}$$

from previous

$$C_v = \frac{C_{v0}}{(1+V_t/\phi)^{1/3}} \quad \& \quad \frac{dC_v}{dV_t} = \frac{C_{v0}}{3\phi(1+V_t/\phi)^{4/3}}$$

$$\therefore \frac{d\omega}{dV_t} = \frac{C_d^2}{\omega \cdot L \cdot C_{v0} (C_s+C_d)^2 3 \cdot \phi (1-V_t/\phi)^{2/3}}$$

= previous result scaled by $\frac{C_d^2}{(C_s+C_d)^2}$

Want to reduce varactor size by factor 3, but keep the same KVCO at 1.2256Hz.

$$\Rightarrow \frac{C_d^2}{(C_s+C_d)^2} = \frac{1}{3}$$

$$\Rightarrow C_d = 1.37 . C_s .$$

$L = 5n$, $C_T = 3.38pF$ (1.225 GHz). $C_v = 16pF$. (@1V Vt).

$\Rightarrow C_s = 1.53pF$. $\Rightarrow C_d = 2.10pF$.

in previous circuit $\Rightarrow C_s = 3.1p$. $C_d = 4.2pF$.

---

if L is at +10%, Cs at +10%. (process exchange) Cv same.

What is value of Cd and KVCO? (for 1.2256Hz)

New $C_T = 3.07pF$. , $C_s = \frac{3.4pF}{2}$, $C_v = 16pF$.

$\Rightarrow C_d = 1.53pF$ $\left(\times 2 = 3.07pF.\right)$

$\frac{\partial \omega}{\partial t} = \times \frac{1}{1.1}$ (inductor) $\times \frac{0.224}{0.333} \leftarrow \frac{C_d^2}{(C_s+C_d)^2}$ ratio. $= \times \underline{\underline{0.61}}$ of previous ratio.

61% of KVCO

(was $\Rightarrow 0.62$).

repeat L at -10%, Cs at -10%.

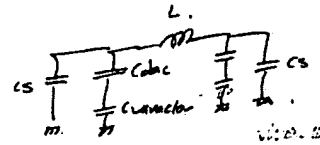
New C_T (for 1.225GHz) is 3.75pF, $C_s = 1.4pF$, $C_v = 16pF$.

$\Rightarrow C_d = 2.75pF$ $\left(\times 2 = 5.5pF\right)$.

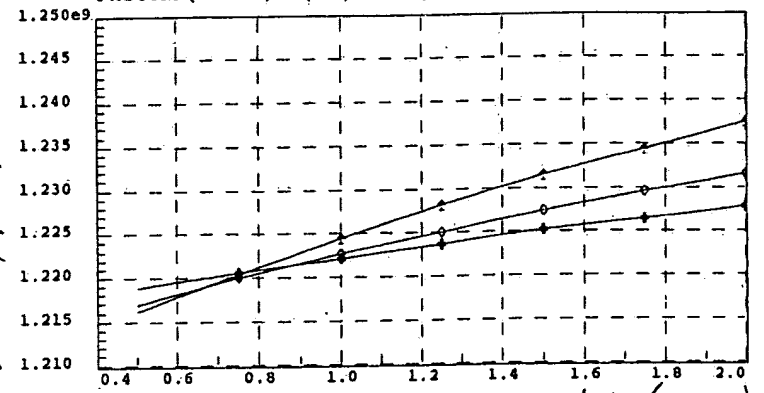
$\frac{\partial \omega}{\partial t} = \times \frac{1}{0.9} \times \frac{0.439}{0.333} = \times 1.47$

147% of KVCO.

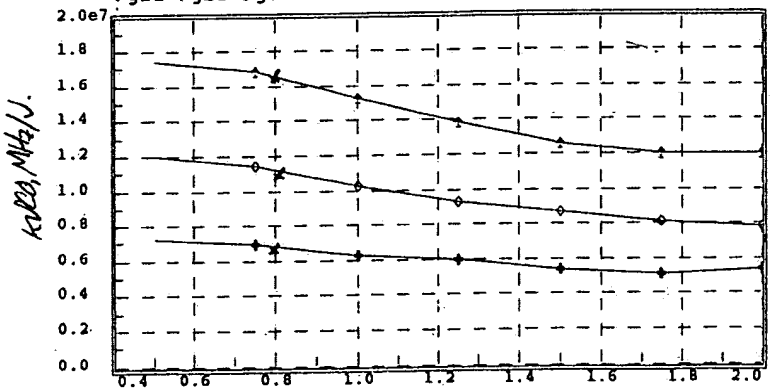
Results are:



◇XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_1:9 5n, Cs = 3.1p Cdac = 4.2p.
♦XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_2:9 5.5n, Cs = 3.4p Cdac = 3.05p.
‡XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_3:9 4.5n, Cs = 2.8p Cdac = 5.6p.



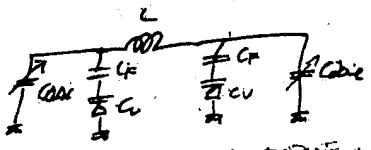
◇gr1 ♦gr2 ‡gr3



7 → 17 MHz/V.

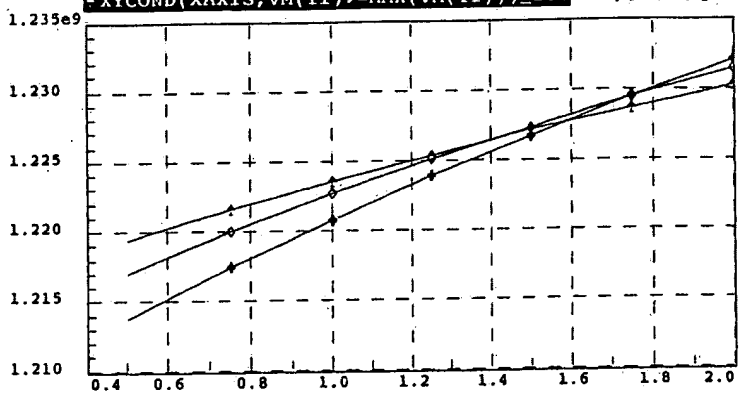
Simulation shows variation in KVCO for process tolerance of inductance and capacitance, Cs large by 10% for inductance large by 10%. + ditto for -10%.

KVCO variation too large.

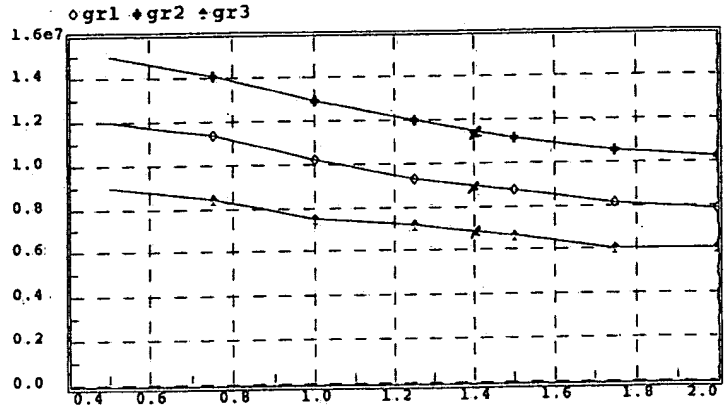


$C_J = 220fF$

◇XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_1:1 L=5n C_F=4.2p Cable=3.1p.
◆XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_2:1 L=5.5n C_F=4.8p Cable=2.2p.
◈XYCOND(XAXIS,VM(T1)>=MAX(VM(T1)))_3:1 L=4.5n C_F=3.8p Cable=4.15p.



◇gr1 ◆gr2 ÷gr3



7 → 11.5 MHz/V.

Repeat of previous except fixed capacitance in series with varactor. Capacitance and tolerance tolerance swept together for worst case. Variation in VCO should be reduced.

Final VCO Trim tolerance. 22 March 99.

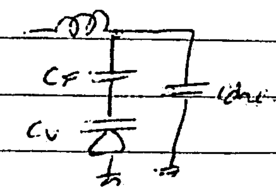
Want KVCO ≥ 10 MHz/V. at 1.225 MHz. Single Varactor per side

previous tolerance ⇒ 8-12 MHz/V with process.

C varactor ≥ 16 pF at 1V Vreverse.

Fixed capacitor in with varactor, Cdac to gnd.

Want Varactor voltage within 0.6 V.



0.6 × 8 MHz/V ⇒ Cdac to trim to nearest 4.8 MHz.

From previous page for 10 MHz/V, $C_F = 3.3\,pF$ ≐ Cdac.

SnH requires 3.38 pF total ⇒ 6.76 pF (2 in series).

$C_F = 3.3\,pF$.

⇒ C_F ser C_v = 2.7 pF.

(nom). ⇒ Cdac = ~~3.83~~ 4.0 pF. nom.

$$\frac{\partial f}{\partial C_{dac}} = \frac{1}{C_T^2 \cdot \omega \cdot L \times 2\pi} = \frac{90\,MHz}{pF}$$

to nearest 4.8 MHz ⇒ ΔCdac = 0.053 pF.

Dac range.

C = +10% } ⇒ C_T = 6.14 pF, ⇒ (C_F = 3.6 pF) Cdac = ~~2.7~~ pF. 3.2 pF.
L = +10% }

C = −10% } ⇒ C_T = 7.44 pF ⇒ (C_F = 3.0 pF) Cdac = ~~4.7~~ pF. 4.9 pF
L = −10% }

Cdac has same ±10%.

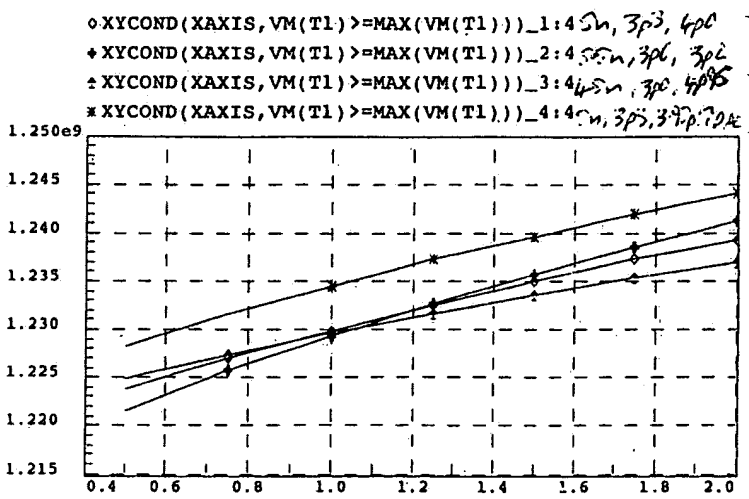
⇒ ~~3.2~~ 2.9 → ~~5.2~~ 5.4 pF in 0.053 pF steps. ~ nom.

⇒ Dac = 2.7 pF + (0→63) × 45 fF steps

↓

try ~~2.8~~ 2.7 pF + (0→63) × 50 fF steps

Results with previous values. (5 pF varactor, 1 pole).

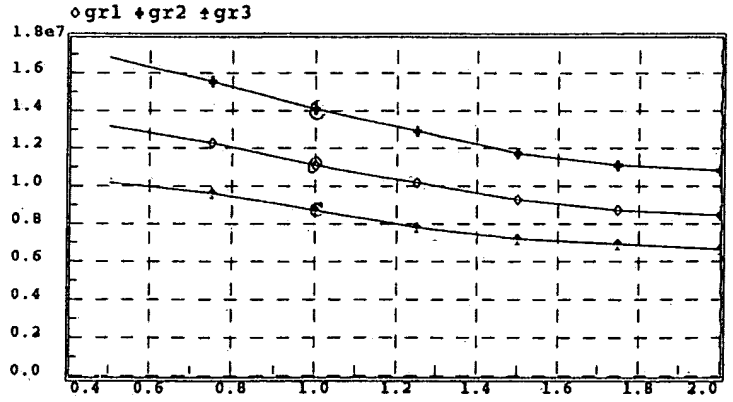


→ trace = circuit at MHz/pF

≈ 5 MHz / 50 fF.

= 100 MHz / pF.

(calculated 90).



9-7 ≈ 4 MHz/V.

Assume L = 120 nH.

⇒ C_T from 5.6 to 8.1 pF.

⇒ C_{die} from 2.6 to 5.6 pF. ± 10% ⇒ nominal from 2.4 to 6.2 pF.

in 6 steps ⇒ max 60 fF / step

⇒ max ± 66 fF / step.

⇒ ΔV_{tune} of $\frac{6\ MHz}{9\ MHz/V}$

= 0.67 V

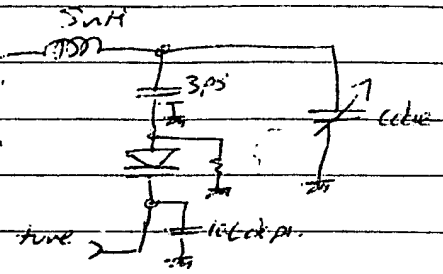
⇒ 0.3 ⇒ 1.5 V.

Simulations suggest 2.2 pF + (0.763) × 70 fF.

(high ⇒ 2.6 pF varied ⇒ 2.2 nom.)

Trim network for VCO.

Varactor $C_j \approx 25pF$ device with 3.3pF cap in parallel with DAC, 6 bit word 2-2 → 6.6pF, ~~70fF~~ LSB max. x 2 off, one on each side of Pierce circuit.



Cdac: Q > 20 at 1.2256MHz.

assume resistance dominated by fet, 70fF max → 77fF max.

$R_{SW} < 80\Omega$.

$\Rightarrow \frac{W}{L} > 160$ say 200 $\Rightarrow \frac{W}{L} = \frac{18}{.35}$.

$C_{off} \approx 10 \to 20\mu F$

$\Rightarrow$ unit = ~~100~~ 90fF to give > of ~~320~~ fF.

Build from 150fF units + divide LSB

Testchip - Bicmos.
Wk 16 → tape out (3½ wks away).
Wk 18 → process start.

Charge Pump: - 250μA full switch.

---

30 March 99.

VCO resize.

Assume inductance of 4.9nH has ∓20% tolerance and Q of 5 ±20%. ⇒ Model as variable L, fixed R.

Cdac has Q ≥ 15.

typical case: pierce gm > 10.5mA/V for gain ≥ 1.
(excluding Q of CDAC)

low q case pierce gm ≥ 17mA/V
(including Q of CDAC)

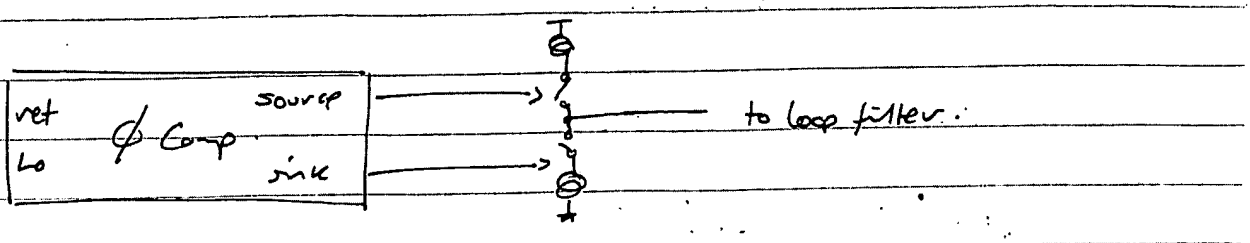
max q case. pierce gm ≥ 7.3mA/V.
(excluding Q of CDAC)

Drive device sizes, require gm·Zc (gain) ≥ 1.5 for osc.
aim for gain ≥ 2.
⇒ each device to handle gm quoted above.

Assuming K' from 100→200 μA/V
ΔV of 0.4V max, gm 17mA/V
⇒ $\frac{220}{.35}$ Nch at ≈5mA.

Sims ⇒ OK.
See ~ testchip/marsail/schematics/ars/analogue/...

Synth output pad - phase comparator and charge pump. 31 March 99.



Phase comparator, test digits, essentially two D-type comparators formed from ~~~~ NAND gates. Reset signal applied directly to outputs as opposed to standard scheme where only 'ripples' through D-types. Reset pulse causes both outputs to become active - extended to allow current sources to switch cleanly hence reduce deadband (0 phase offset) problems.

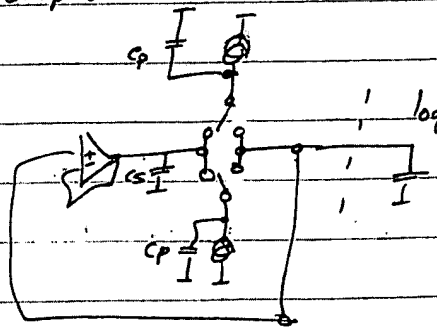
i.e. structure developed on 'Page-in-a-book' project.

Charge pump output:

to minimise current due to charging/discharging parasitic capacitances of current sources, and reverse turn-on/off times of current sources, leave current sources on and minimise voltage change across them during switch.

Two standard approaches.

i, Buffer output voltage and switch currents to this also not switched to output.



Whereby current source is switched to the output the voltage across the current sources is largely unchanged. ΔV small $\Rightarrow$ I_{SW} with small. Also turn off - turn on - turn off turn on sequence on switches to give similarly small internal output output internal switching current due to charge injection (staged degree of cancellation).

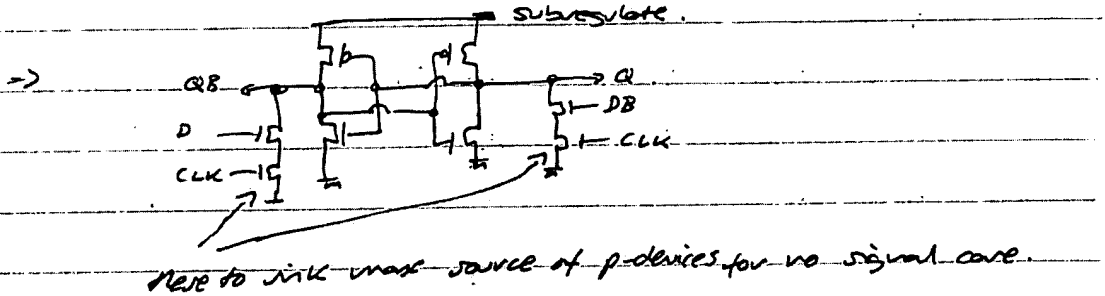
12-April-99.

Prescaler.

Fast divider:- Tried scheme.

idea. Forward latch from two cross coupled inverters. Set the current in these by reverse biasing their supply voltage.

Drivers biased such that at quiescent it can still sink as much current as the p-device sources.



÷64/65.

As previously used follow a dual modulus 4/5 with a divide by 16 and decode logic such that 4/5 may only divide by 5 in one state of the 16.

-ve edge faster ⇒ use -ve edge as trigger between blocks and at output.

Want maximum set-up time for modulus control ⇒ last slot of 16 before output changes, also required to have 4/5 decide if doing a 4 or 5 divide on its state immediately before its output changes. (÷5 with add pulse after output has changed.)

20 April 99.-

Information required from S.T.

1, Layout related for test chip on b.icmos.

a, Details of protection structures + requirements for pad cells which use driver devices which are with a pad.

is an example analogue output pad / input pad available in both schematic (+CDL) + layout form.

b, Details of supply protection scheme + cells (layout, CDL + schematic) for use on test chip.

c, Digital cells - ST to place, or
or - us to place but require layout and CDL of cells.
- library details.

2, General

a, Process details.
require Inductors; Poly-poly capacitors; RL-pinbase resistors and standard devices from HCMOS6. Please confirm.

b, Documentation. We have:- Bicmos design rule manual, 0073470 rev C.
HCMOS6 design rule manual, 0090966, rev C.
Model kit , CDR96-043, rev E.
Are these up to date?
Have seen (Fat folder) STKM6000 rev 2.0.
library reference manual. - circuits + specs ✓
- functions + specs.
0.35um libraries user manual, rev 1.0

c, Netlist - i, CDL format.
ii, layout devices to be included? Nd/s with protection gate capacitance wires...

Eldo → L-Edit netlist conversion. 7-May-99.

Currently all components are subcircuit calls to subcircuits which map onto primatives, eldo does the mapping.

For L-Edit, need to either define a mapping - can it handle passing parameters? or convert the netlist.

Convert netlist is probably easiest.

Rules:

'X_' removed.

'NFING' → '$ NFING'.

~~it would also want to replace~~ 'W=' by '$W=' for resistors and capacitors.

↓ resistors and capacitors → + third terminal to be removed.

Tool Navig Meeting - 10 May 99.

NDA - sort art out with Paul Egan

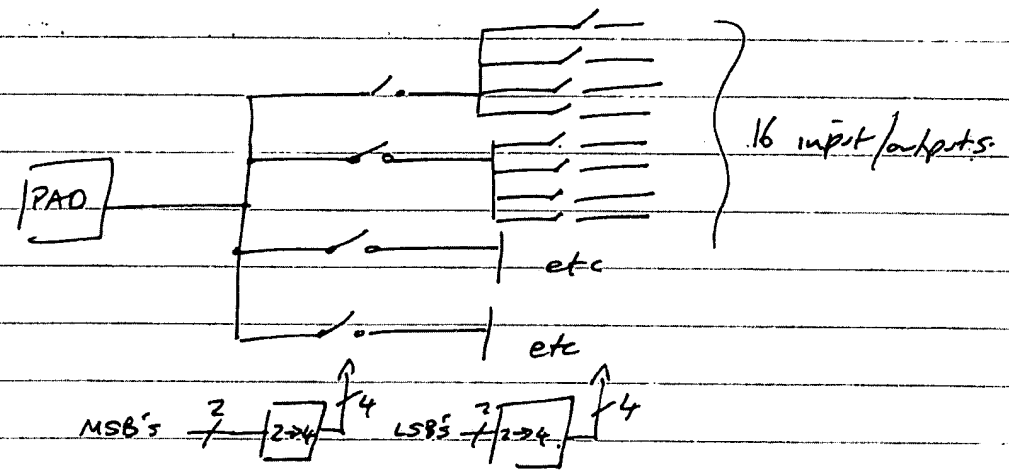
Sort art pads (analogue in font) + supply protection.
+ hole for digits - with parts.

VCO - need to finish - beg as probs of amplitude problem.

Analogue multiplexer pad. ANMX_PAD. 20 May 99.

During layout final design was too large to fit in a standard pad outline and required a wider pad width. Pads very tight.
Design based upon 4→16 decoder and 16 analogue switches.

For future build with two 2→4 decoders and two sets of analogue switches in series. ⇒ less gates + less routing signals (control signals).



⇒ factor of 2 increase in switch resistance (for same size devices in analogue switches)

Toothfairy test chip on ST BiCMOS process 17 June 1999.
virtually complete.

Parts worth Noting:-

Bicmos layers used:-

NWELL ONLY in VARACTOR DIODES.
(explicit). BURIED_N+ in VARACTOR DIODES.
SINKER in RF PADS and VARACTOR DIODES.

HCMOS 6 cells. (modified).

VSS protection diodes. } All modified in Metal
Vdd protection (MOSSWT protection) cell. } layers.
~~Analogue pads~~

Modified Bicmos6 cells.

Analogue pads DP diodes have had BuriedN, Sinker and
Nwell only layers removed.
NOTE: these diodes are larger area than the HCMOS6
equivalent.

Two tone distortion products (again) 15 July 99.

Two tone input, two tones at different frequencies and amplitudes.

Input = $A\cos\omega_1 t + B\cos\omega_2 t$, response $x + \alpha x^3$.

reminder
$\cos(A+B) = \cos A\cos B - \sin A \sin B$.
$\cos(A-B) = \cos A\cos B + \sin A \sin B$

$\Rightarrow$ output = $(A\cos\omega_1 t + B\cos\omega_2 t) + (A\cos\omega_1 t + B\cos\omega_2 t)^3$

expand $\Rightarrow$ $\cos\omega_1 t\left[A + \alpha A^3\frac{3}{4} + \alpha\frac{3}{2}B^2A\right] + \cos 2\omega t\left[B + \frac{3B^3}{4}\alpha + \frac{3}{2}\alpha A^2 B\right]$.

$+ \cos 3\omega_1 t\left[\frac{3A^3\alpha}{4}\right] + \cos 3\omega_2 t\left[\frac{3B^3\alpha}{4}\right]$.

$+ \frac{3}{4}\alpha A^2 B\left[\cos(2\omega_1 - \omega_2)t + \cos(2\omega_1 + \omega_2)t\right]$

$+ \frac{3}{4}\alpha B^2 A\left[\cos(2\omega_2 - \omega_1)t + \cos(2\omega_2 + \omega_1)t\right]$.

Our system:- At first filter have : centre = 1.5MHz.

ω_1 = 1st adjacent at 2.5MHz

ω_2 = 2nd adjacent at 3.5MHz.

$\Rightarrow$ $2\omega_1 - \omega_2$ case important.

Rectifier structure is current driven, distortion is dependant upon the signal levels throughout the circuit. $\Rightarrow$ a less linear structure ~~is~~ a structure which has reduced signal levels will have similar overall performance to a structure with good linearity and large signals throughout. Filtering of off channel interferers increases throughout the filter $\Rightarrow$ less amplitude due to attenuation hence lower signal levels.

Distortion Continued:- 21/4/94.

Reran at 'filt1-gm1.in' modelling program. This is distortion at output due to non-linear gm1 for the basic filter structure, we are with similar input and output levels.

Inputs:- , on channel -85dBm => 2mV pk.

Passive filter, 1st order at 2.5MHz.

-39dBm tones { 1st tone 4.5MHz 0.36V pk => 1.73mV pk after passive
2nd tone 7.5MHz 0.36V pk => 812mV pk after passive.

generates 116μV pk at filter out for $\alpha = 0.5$ in gm1.

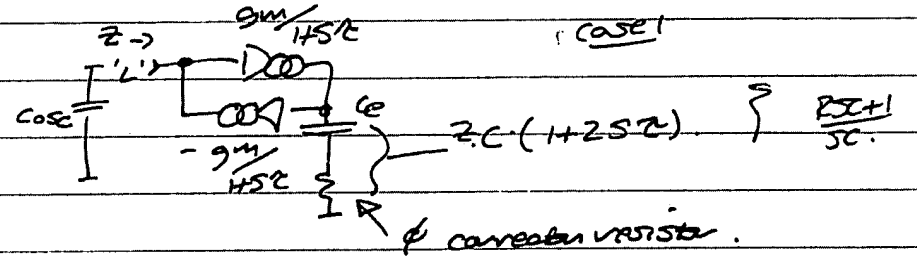
=> If this is the worst case, and transconductor elements always have $\alpha < 0.5$ can use a basic filter structure - better for noise - and achieve linearity spec.

↓

Noise improvement < 1dB. => go with more linear filter.

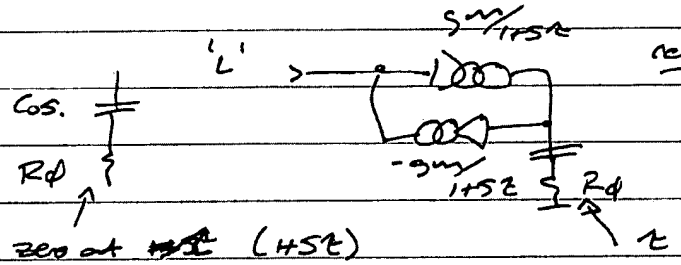
Filters: Passive phase compensation. 26 July 99.

'Page' filters were single ended. Pole caused by current mirror in transconductor altered transfer function, could be tuned out in filter component value choice but then the filter response varied unacceptably over process. Solution was to add a zero to the emulator capacitor, i.e. phase correct the inductor emulator section.



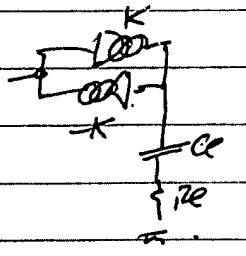
case 1

Alternative is to compensate for φ at one gm only and multiply response by (1+sτ).



case 2.

Analysis of above:—



$$\frac{V_1}{i_1} = \frac{s.Ce}{K^2(1+sCeRe)}. \qquad K = \frac{gm}{1+s\tau_g}.$$

$$\Rightarrow \frac{V_1}{i_1} = \frac{sCe\,(1+s\tau_g)^2}{gm^2.(1+s.Ce.Re)}.$$

case 1 $Ce.Re = 2\tau_g$.

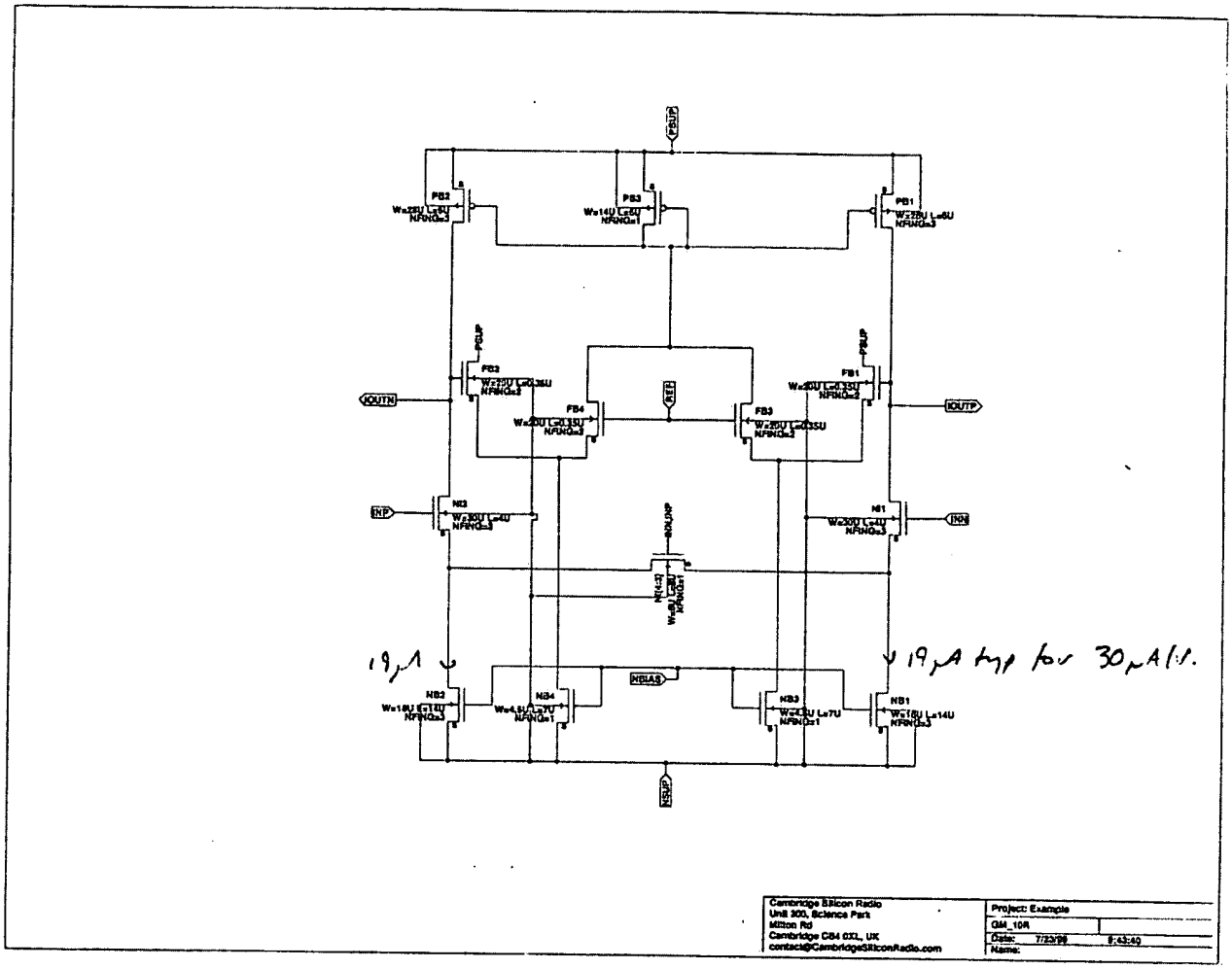
$$\Rightarrow \frac{s.Ce}{gm^2} + \frac{s^3\tau^2 Ce}{gm^2(1+s.2\tau_g)}.$$

case 2

$$Ce.Re \simeq \tau_g. \simeq \frac{sCe(1+s\tau_g)}{gm^2}.$$

Filter transconductance amplifier. 28/4/99.

Differential in, differential out with set point for output level.

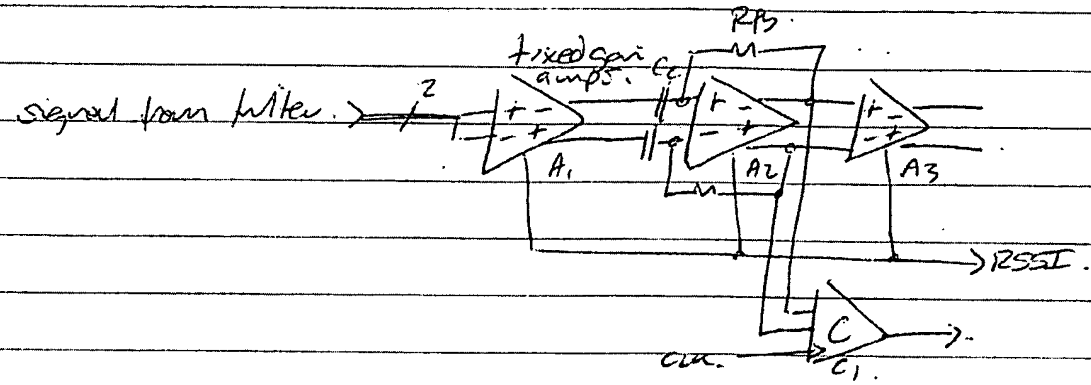


Require 2% gm matching, single spring for acceptable filter response. Were multiple transductors placed in parallel get x% transductance with $\sqrt{x}$ x variation. Hence get $\sigma_{gm} < 2\%$ for typical processing on one transductor, should have some margin for typical process filter. Target is $\sigma_{gm} < 7\%$ over all process.

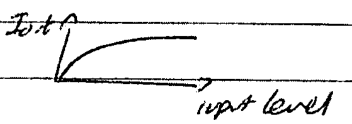
Expect better matching possible from Cap elements, so aim for 2% but accept best possible and correct in Cap elements.

Circuit above has been designed for low noise and high linearity, therefore most of its devices have large ($V_{GS} - V_T$) values, this is good for matching $\Rightarrow$ check σ_{gm} for above and correct if necessary.

Detector Circuitry (Timing Diagram). 12 Aug 98



fixed low gain limiting amps have limit output which generates a current when a signal input threshold is crossed, ⇒ output current is inverse rise in shape, i.e.



pseudo log.

Want fast comparator, for low effective input offset and low current ⇒ small devices in comparator (good BW for low current) preceded by gain (reduce input offset).

AC gain arrangement above ⇒ offsets of C_1 and A_2 and bit are divided by gain ($A_1 \times A_2$). Hence for input offset of $\leq$ 0.4mV and gain per stage at 6, offset can be as high as 14.4mV!

Required output is 4 bit word, previous four samples of a 4 phase clock. MSB to be ~~first~~ most recent sample. Data Rate 16MHz (4 bits).

⇒ either one comparator at 64MHz or 4 comparators at 16MHz.

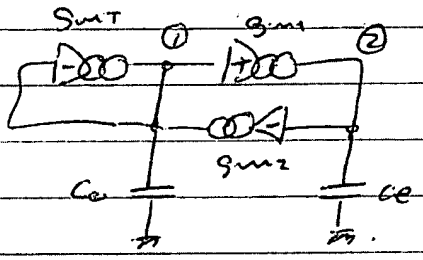
Current consumption not linear with frequency (especially with logic for generating fast strobe signals) ⇒ choose 4 comparator option.

All pass filter (update). 31 Aug 99.

require transfer function of form

$$\frac{s^2 - bs + c}{s^2 + bs + c}.$$

Consider:-



NAM. =	1	2
1	$g_{mT} + sC_e$	g_{m2}
2	$-g_{m1}$	sC_e

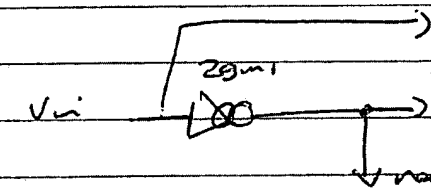
$$Z_{11} = \frac{sC_e}{s^2 C_0 C_e + sC_e g_{m1} + g_{m1} g_{m2}}$$

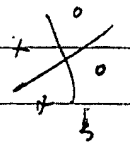
$$\therefore \quad 1 - 2g_{m1} \cdot Z_{11} = \frac{s^2 C_0 C_e - g_{m1} s C_e + g_{m1} g_{m2}}{s^2 C_0 C_e + g_{m1} \cdot s \cdot C_e + g_{m1} g_{m2}}$$

$$= \text{all pass.}$$

$\Rightarrow$ drive node 1 with a current and monitor voltage difference between input voltage / $2g_{m1}$ and V_1.

i.e.

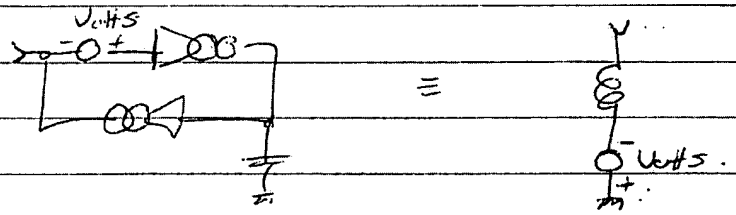




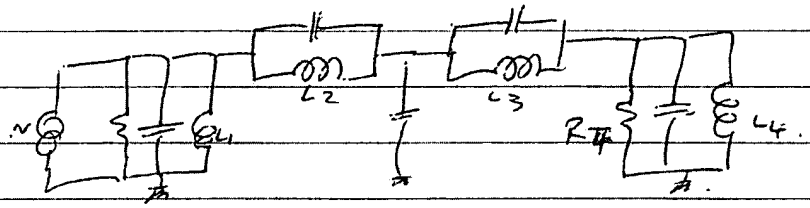
DC. correction circuit :-

7 Sept.

The 2-5MHz bandpass filter contains four inductors in a ring. The gyr-C inductor realisation of an inductor contains an offset voltage due to offset voltages in the transconductors which form it :-



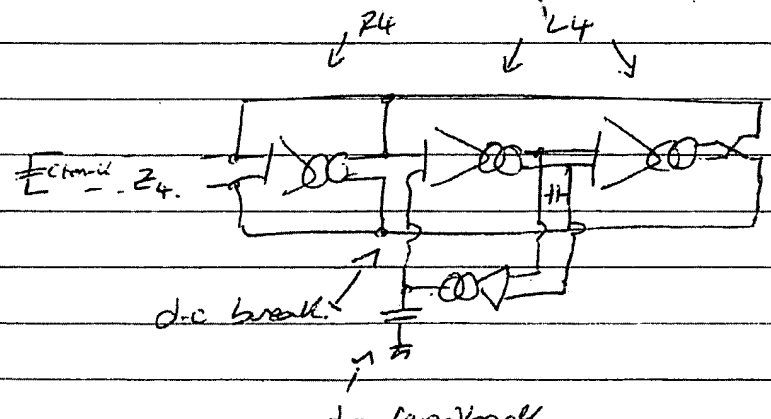
Filter Structure :-



⇒ Need dc break in L_1, L_2, L_3, L_4 loop.

Put d-c block in L_4 :-

$L_4 + R_4$. with d.c. block.



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